METHOD OF CONTROLLING AN ELECTRONIC NON-VOLATILE MEMORY AND ASSOCIATED DEVICE

Abstract of the Disclosure

A memory cell in an EEPROM includes a floating gate transistor that includes a first conducting terminal and a control gate. A method of controlling the memory cell includes setting a state of the memory cell by simultaneously applying voltage pulses of opposite polarities respectively to the first conducting terminal and to the control gate. The voltage pulses including a first portion having a first slope and a second portion having a second slope, wherein the second slope is based upon the polarities of the voltage pulses. The method allows the amplitude of the voltage pulses to be reduced.